

IN THE CLAIMS

Claims 1-54 (Previously Cancelled)

55. (Currently Amended) A semiconductor structure comprising:
a monocrystalline silicon substrate;
an amorphous oxide material in contact with the monocrystalline silicon substrate;
a monocrystalline metal oxide ~~or metal nitride~~ layer overlying the amorphous oxide material;
a metal capping layer in contact with said metal oxide or metal nitride layer;
a compound semiconductor template layer in contact with said capping layer;
and;
a monocrystalline compound semiconductor material in contact with said template layer,

wherein the monocrystalline compound semiconductor material is piezoelectric, and wherein the monocrystalline compound semiconductor material thickness is between about 0.5 μm and 10 μm .

56. (Original) The semiconductor structure of claim 55 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

57. (Original) The semiconductor structure of claim 55 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

58. (Currently Amended) A semiconductor structure comprising:
a monocrystalline silicon substrate;
an amorphous oxide material in contact with the monocrystalline silicon substrate;
a monocrystalline metal oxide ~~or metal nitride~~ layer overlying the amorphous oxide material;
a metal capping layer in contact with said metal oxide or metal nitride layer;

a compound semiconductor template layer in contact with said capping layer;
and;

a monocrystalline compound semiconductor material in contact with said template layer, wherein the monocrystalline compound semiconductor material is piezoelectric, and

wherein the monocrystalline compound semiconductor material creates a reflective surface.

59. (Original) The semiconductor structure of claim 58 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

60. (Original) The semiconductor structure of claim 58 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

61. (Original) The semiconductor structure of claim 58 wherein the monocrystalline compound semiconductor material thickness is between about 0.05 μm and 100 μm .

62. (Original) The semiconductor structure of claim 58 further comprising an integrally formed electrical component in communication with the reflective surface of the monocrystalline compound semiconductor material.

63. (Currently Amended) A semiconductor structure comprising:
a monocrystalline silicon substrate;
an amorphous oxide material in contact with the monocrystalline silicon substrate;
a monocrystalline metal oxide or metal nitride layer overlying the amorphous oxide material;
a metal capping layer in contact with said metal oxide or metal nitride layer;
a compound semiconductor template layer in contact with said capping layer;
and;

a monocrystalline compound semiconductor material in contact with said template layer, wherein the monocrystalline compound semiconductor material is piezoelectric,

further comprising a reflective material overlying the monocrystalline compound semiconductor material.

64. (Original) The semiconductor structure of claim 63 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

65. (Original) The semiconductor structure of claim 63 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

66. (Original) The semiconductor structure of claim 63 wherein the monocrystalline compound semiconductor material thickness is between about 0.05 μ m and 100 μ m.

67. (Original) The semiconductor structure of claim 63 further comprising an integrally formed electrical component in communication with the reflective material overlying the monocrystalline compound semiconductor material.

68. (Currently Amended) A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material in contact with the monocrystalline silicon substrate;

a monocrystalline metal oxide ~~or metal nitride layer~~ overlying the amorphous oxide material;

a metal capping layer in contact with said metal oxide or metal nitride layer;

a compound semiconductor template layer in contact with said capping layer;

a monocrystalline compound semiconductor material in contact with said template layer, and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material,

wherein the piezoelectric monocrystalline semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide, and

wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.05 μm and 10 μm .

69. (Currently Amended) A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material in contact with the monocrystalline silicon substrate;

a monocrystalline metal oxide or metal nitride layer overlying the amorphous oxide material;

a metal capping layer in contact with said metal oxide or metal nitride layer;

a compound semiconductor template layer in contact with said capping layer;

a monocrystalline compound semiconductor material in contact with said template layer, and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material,

wherein the piezoelectric monocrystalline ceramic material is selected from the group consisting of barium titanate, lead titanate, potassium niobate, lead niobate, and lead zirconate titanate, and

wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.5 μm and 200 μm .

70. (Original) The semiconductor structure of claim 69 wherein the piezoelectric ceramic material thickness is between about 5 μm and 25 μm .

71. (Currently Amended) A semiconductor structure comprising:

an amorphous oxide material in contact with the monocrystalline silicon substrate;

a monocrystalline metal oxide or metal nitride layer overlying the amorphous oxide material;

a metal capping layer in contact with said metal oxide ~~or metal nitride layer~~;
a compound semiconductor template layer in contact with said capping layer;
a monocrystalline compound semiconductor material in contact with said template layer; and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material creates a reflective surface.

72. (Currently Amended) A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material in contact with the monocrystalline silicon substrate;

a monocrystalline metal oxide ~~or metal nitride layer~~ overlying the amorphous oxide material;

a metal capping layer in contact with said metal oxide or metal nitride layer;

a compound semiconductor template layer in contact with said capping layer;

a monocrystalline compound semiconductor material in contact with said template layer, and

a piezoelectric material overlying the monocrystalline compound semiconductor material,

further comprising a reflective material overlying the piezoelectric material.

73. (Original) The semiconductor structure of claim 71 further comprising an integrally formed electrical component in communication with the reflective surface of the piezoelectric material.

74. (Original) The semiconductor structure of claim 72 further comprising an integrally formed electrical component in communication with the reflective material overlying the piezoelectric material.

Claims 75-90 (Previously Cancelled).